				ATTY DOOUTE NO		ADDUCATION	Page 1 of 10
							10/815,742
ı	FORM F	PTO-1449		FIRST NAMED INVENTOR		To be Assigned	10/815, 142
=				WANG et al.			
MATION	DISC	LOSURE ST	ATEMENT	FILING DATE ART UNIT			
						To Be Assigned	
	IDOC	LIMENT	U.S. PA	ATENT DOCUMENTS		<u>-</u>	
			DATE	NAME	CLASS	SUB-CLASS	FILING DATE
AA1			12/02/1986	Torii	100.00	300-00-33	FILING DATE
					-	` -	—
AB1		-	06/23/1987	Uchida	_		
AC1	4,72	2,049	01/26/1988	Lahti	_	-	_
AD1	4,80	7,115	02/21/1989	Torng			
AE1	4,82	3,201	04/18/1989	Simon et al.			
AF1	4,90	3,196	02/20/1990	Pomerene et al.	_		
AG1	4,94	2,525	07/17/1990	Shintani et al.			
AH1	5,06	7,069	11/19/1991	Fite et al.			
Al1	5,07	2,364	12/10/1991	Jardine et al.		_	
AJ1	5,10	9,495	04/28/1992	Fite et al.			_
AK1	5,12	25,083	06/23/1992	Fite et al.			
٠			FOREIGN	PATENT DOCUMENTS			<u> </u>
Τ-	DOC	UMENT	TORLION	TATENT BOCOMENTS	7	- 1	γ
			DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
AL1	wo	88/09035	11/1988	PCT WIPD			Yes No
AM1	0 51	5 166	11/1992	EPO EPO	_		Yes No
AN1	H2-4	18732	02/19/1990	Japan		-	Yes No
<u> </u>		OTHER (ncluding Auth	or, Title, Date, Pertinent P	Pages, et	(c.)	I NO
AO	1	Acosta, R. D. o	et al., "An Instruction On Computers, IEEE	n Issuing Approach to Enhancing Perf , Vol. C-35, No. 9, pp. 815-828 (Septe	formance in ember 1986)	Multiple Functional Ur	nit Processors," IEEE
AP	1	Agerwala, T. a 31, 1987).	and Cocke, J., "High	Performance Reduced Instruction Sct	Processors,	BM Research Division	on, pp. 1-61 (March
AR	1	Butler, M. and Ann Arbor, M	Patt, Y., "An Improichigan, 24 pages (Ja	roved Area-Efficient Register Alias Table for Implementing HPS," University of Michigan, (January 1990).			
AS	1	Butler, M. et a Symposium on	I., "Single Instruction Computer Architect	n Stream Parallelism Is Greater than T ure, ACM, pp. 276-286 (May 1991).	`wo," <i>Proced</i>	edings of the 18 th Annu	al International
ĂT`	1	Charlesworth, Computer, IEE	A.E., "An Approach E, Vol. 14, pp. 18-2	to Scientific Array Processing: The A7 (September 1981).	rchitectural	Design of the AP-1'201	B/FPS-164 Family,"
		Ellis					10/14/2004
al if refere d. Includ	ence co le copy	nsidered, whet of this form wit	her or not citation i th next communica	s in conformance with MPEP 609. tion to Applicant.	Draw line	through citation if no	t in conformance
	AA1 AB1 AC1 AC1 AF1 AG1 AH1 AH1 AH1 AN1 AC1 AC1 AC1 AC1 AC1 AC1 AC1 AC1 AC1 AC	AA1 4,67 AA1 4,67 AA1 4,67 AC1 4,72 AD1 4,80 AE1 4,90 AG1 4,94 AH1 5,06 AH1 5,07 AJ1 5,10 AK1 5,12	DOCUMENT NUMBER AA1	DOCUMENT NUMBER DATE	MATION DISCLOSURE STATEMENT	SP038.CS (1397.0140005) FIRST NAME NAMS et al. FILING DATE April 2, 2004	SP038.CS (1387.0140005) To Be Assigned

248134_1.DOC

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

	Page 2 of 10
ATTY. DOCKET NO.	APPLICATION NO.
SP038.C5 (1397.0140005)	To Be Assigned 10/8/5,742
FIRST NAMED INVENTOR	
WANG et al.	
FILING DATE	ART UNIT
April 2 2004	To Ro Assigned

				U.S. P	ATENT DOCUMENTS			
EXAMINER			UMENT		T.			
INITIAL	AA2	5,148		DATE 09/15/1992	NAME Witek et al.	CLASS	SUB-CLASS	FILING DATE
RUE		<u> </u>	-	09/13/1992	Witek et al.	~		
RUE	AB2	5,167	<u> </u>	11/24/1992	Murray et al.		_	
RUE	AC2	5,179	,673	01/12/1993	Steely, Jr. et al.			
RUE	AD2	5,197	,132	03/23/1993	Steely, Jr. et al.		,	_
RUE	AE2	5,214	,763	03/25/1993	Blaner et al.			1 ~
RUE	AF2	5,222	2,240	06/22/1993	Patel		-	
RIE	AG2	5,226	,126	07/06/1993	McFarland et al.	1		
RIE	AH2	5,230	,068	07/20/1993	Van Dyke et al.	-		1
RUE	Al2	5,251	,306	10/05/1993	Tran			
RE	AJ2	5,317	,720	05/31/1994	Stamm et al.	_		_
RUE	AK2	5,345	,569	09/06/01994	Tran			† ~
	-	·	· · ·	FOREIGN	PATENT DOCUMENTS			<u> </u>
EXAMINER INITIAL		DOCUMENT NUMBER		DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
RLE	AL2	H4-9	96132	03/27/1992	Japan			Yes No
RLE	AM2	H6-	19707	01/28/1994	Japan	_	_	Yes No
	AN2							Yes
	,		OTHER (Including Aut	hor, Title, Date, Pertinen	t Pages, etc.)	' <u></u>	
RUE	AO	2	Colwell, R.P.	et al., "A VLIW Are ral Support for Prog	chitecture for a Trace Scheduling Coramming Languages and Operating	ompiler," <i>Proceedi</i> g <i>Systems</i> , ACM, pp	ngs of the 2nd Interp. 180-192 (Octobe	rnational Conference r 1987).
RIE	АР	2	Dwyer, H, A	Multiple, Out-of-Ord	ler Instruction Issuing System for Su	sperscalar Processo	ors, UMI, pp. 1-249	9 (August 1991).
RUE	AR	2	Foster, C.C. and Riseman, E.M., "Percolation of Code to Enhance Parallel Dispatching and Execution," <i>IEEE Transactions On Computers</i> , IEEE, pp. 1411-1415 (December 1971).					
RIE	AS	<u>2</u>	Gee, J. et al., "The Implementation of Prolog via VAX 8600 Microcode," Proceedings of Micro 19, IEEE, October 1986, pp.68-74.					
RLE	AT	2	Gross, T.R. and Hennessy, J.L., "Optimizing Delayed Branches," Proceedings of the 5th Annual Workshop on Microprogramming, IEEE, pp. 114-120 (October 5-7, 1982).					
EXAMINER -	Pichar					1	CONSIDERED	10/14/2004
EXAMINER: Init and not consider	ial if refer ed. Inclu	ence co de copy	nsidered, whe	ether or not citation ith next communication	is in conformance with MPEP 60 ation to Applicant.	09. Draw line thro	ough citation if no	t in conformance
RUE RUE RUE XAMINER T	AP AR AS AT	2 2 2	Colwell, R.P. on Architectu Dwyer, H, A: Foster, C.C. & Computers, II Gee, J. et al., 74. Gross, T.R. & Microprogram	et al., "A VLIW Are ral Support for Programmed Riseman, E.M.," EEE, pp. 1411-1415 "The Implementation and Hennessy, J.L., "Comming, IEEE, pp. 114	Percolation of Code to Enhance Par (December 1971). The of Prolog via VAX 8600 Microco Detimizing Delayed Branches," Production of Code to Enhance Particles (December 1971).	ompiler," Proceeding Systems, ACM, pp sperscalar Processor rallel Dispatching a de," Proceedings of the 5th	ngs of the 2nd Interp. 180-192 (Octobe ors, UMI, pp. 1-24) and Execution," IEL of Micro 19, IEEE, Community of Micro 19, IEEE, Commu	No rnational Conference r 1987). 9 (August 1991). EE Transactions On October 1986, pp.68-

		Page 3 of 10
DOCKET NO.	APPLICATION NO.	1

To Be Assigned 10/815,747

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO. SP038.C5 (1397.0140005) FIRST NAMED INVENTOR WANG et al. FILING DATE April 2, 2004 ART UNIT To Be Assigned

1				U.S. F	ATENT DOCUMENTS				
EXAMINER			UMENT						
INITIAL	AA3	NUM		DATE	NAME	CLASS	SUB-CLASS	FILING DATE	
KUE		5,355	·	10/11/1994	Shebanow et al.		-		
RUE	AB3	5,367	7,660 	11/22/1994	Gat et al.			_	
RUE	AC3	5,390),355	02/14/1995	Horst		_	_	
RUE	AD3	5,398	3,330	03/14/1995	Johnson		-		
RUE	AE3	5,430),888	07/04/1995	Witek et al.				
RUE	AF3	5,442	2,757	08/15/1995	McFarland et al.				
RUE	AG3	5,487	7,156	01/23/1996	Popescu et al.	_	_		
RUE	AH3	5,560	0,032	09/24/1996	Nguyen et al.				
RUE	AI3	5,561	,776	10/01/1996	Popescu et at.			-	
RUE	AJ3	5.568	3,624	10/22/1996	Sites et al.	_			
RUE	AK3	5,574	,927	11/12/1996	Scantlin		-	~	
				FOREIGN	N PATENT DOCUMENTS		<u> </u>	<u> </u>	
EXAMINER			CUMENT			-2	T		
INITIAL		NUI	MBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
	AL3							Yes	
	AM3							No Yes	
	1	1				- 		No	
	AN3	Ш.,						No	
·	· 		OTHER (Including Aut	hor, Title, Date, Pertinen	t Pages, etc.)			
RIE	AO	3	Hennessy, J.L 257-278, 290-	Hennessy, J.L. and Patterson, D.A., Computer Architecture: A Quantitative Approach, Morgan Kaufmann Publishers, pp. xi-xv, 257-278, 290-314 and 449 (1990).					
RUE	AP	<u>3</u>	Hwu, W-M. V Computers, II	W. and Patt, Y.N., "CEE, Vol. C-36, No.	Checkpoint Repair for High-Perform 12, pp. 1496-1514 (December 198	nance Out-of-Order 7).	Execution Machine	s," IEEE Trans. On	
RUE	AR	3	Hwu, W. and International	wu, W. and Patt, Y., "Design Choices for the HPSm Microprocessor Chip," Proceedings of the Twentieth Annual Hawaii sternational Conference on System Sciences, pp. 330-336 (1987).					
RLE	AS	<u>3</u>	Hwu, W-M. W	vu, W-M. W. and Chang, P.P., "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," occeedings of the 15th Annual Symposium on Computer Architecture, IEEE, pp. 45-53 (June 1988).					
RCE	AT	<u>3</u>	Hwu, W-M. e Hawaii Intern	Hwu, W-M. et al., "An HPS Implementation of VAX: Initial Design and Analysis," Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences, pp. 282-291 (1986).					
EXAMINER 1	Richar		llis			ı	CONSIDERED	10/14/2004	
EXAMINER: Initiand not consider	tial if referenced. Include	ence co le copy	nsidered, whe of this form wi	ther or not citation ith next communic	is in conformance with MPEP 6 ation to Applicant:	09. Draw line thro	ough ditation if not	in conformance	

		Page 4 of 10
ATTY. DOCKET NO.	APPLICATION NO	
SP038.C5 (1397.0140005)	To Be Assigned	10/815,742
FIRST NAMED INVENTOR		
WANG et al.		
FILING DATE	ART UNIT	
April 2, 2004	To Be Assigned	

				U.S. F	PATENT DOCUMENTS			
EXAMINER INITIAL		DOC	UMENT BER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
RUE	AA4	5,592	2,636	01/07/1997	Popescu et al.			- TIENO DATE
RIE	AB4	5,625,837		04/29/1997	Popescu et al.			
RŒ	AC4	5,627	,983	05/06/1997	Popescu et al.	-		
RUE	AD4	5,630	,149	05/13/1997	Bluhm			
RUE	AE4	5,651	,125	07/22/1997	Witt et al.			
RIE	AF4	5,708	,841	01/13/1998	Popescu et al.			
RUE	AG4	5,768	,575	06/16/1998	McFarland et al.			
RUE	AH4	5,778	,210	07/07/1998	Henstrom et al.		_	1_
ROE	Al4	5,797	,025	08/18/1998	Popescu et al.		1	
RUE	AJ4	5,826	,055	10/20/1998	Wang et al.			
RUE	AK4	5,832	,205	11/03/1998	Kelly et al.			_
<u> </u>		<u> </u>		FOREIG	N PATENT DOCUMEN	TS	<u>.</u> .	
EXAMINER			CUMENT				_	
INITIAL		NUN	MBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
$\overline{}$	AL4							Yes No
	AM4							Yes No
\	AN4						-	Yes No
		,	OTHER (Including Au	thor, Title, Date, Pertin	ent Pages, etc.)		
RŒ	AO	4	Hwu, W-M. a	and Patt, Y.N., "HP!	Sm, a High Performance Restrict E, pp. 297-306 (June 2-5, 1986).	ted Data Flow Architect	ure Having Minim	al Functionality,"
RLE	AP	4	Hwu, W. and	Patt, Y., "HPSm2:	A Refined Single-Chip Microen	gine," HICSS '88, IEEE	,pp. 30-40 (1988).	
RUE	AR	4	IBM Journal	BM Journal of Research and Development, IBM, Vol. 34, No. 1, pp. 1-70 (January 1990).				
RLE	AS	4	Johnson, M. S	ohnson, M. Superscalar Microprocessor Design, Prentice-Hall, pp. vii-xi and 87-125 (1991).				
RLE	AT	4	Johnson, W. M	ohnson, W. M., Super-Scalar Processor Design, (Dissertation), 134 pages (1989).				
	Richar		lis		is in conformance with MPF		CONSIDERED	10/14/2004

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

	Page 5 of 10
ATTY. DOCKET NO. SP038.C5 (1397.0140005)	APPLICATION NO. To Be Assigned 10815,742
FIRST NAMED INVENTOR WANG et al.	
FILING DATE April 2, 2004	ART UNIT To Be Assigned

F				US	PATENT DOCUMENT	re			
EXAMINER	I	DOC	JMENT	J	ALEITI DOCUMENT		1	т	
INITIAL		NUM		DATE	NAME	CLASS	SUB-CLASS	FILING DATE	
RUE	AA5	5,832		11/03/1998	Popescu et al.	•	7	- TIENTO BATE	
RUE	AB5	6,131	,157	10/10/2000	Wang et al.			<u> </u>	
RUE	AC5	6,412	,064	06/25/2002	Wang et al.	-	,		
ROE	AD5	5,961	,629	10/05/1999	Nguyen et al.	-	-		
1	AE5		- /					· · · · · · · · · · · · · · · · · · ·	
1	AF5							-	
	AG5							1	
	AH5						-		
	AI5								
	AJ5								
	AK5								
	•		-	FOREIG	N PATENT DOCUME	ENTS			
EXAMINER INITIAL			CUMENT MBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
. \	AL5							Yes No	
	AM5							Yes No	
\	AN5	i						Yes No	
		,	OTHER (Including Au	thor, Title, Date, Per	tinent Pages, etc.		-	
RUE	AO	<u>5</u>	Proceedings of	and Wall, D.W., "A of the 3rd Internati 2-282 (April 1989)	Available Instruction-Level Paronal Conference on Architecture.	rallelism for Superscalar a ural Support for Program	nd Superpipelined N ning Languages and	Machines," I Operating Systems,	
RIE RIE	AP	<u>5</u>	Keller, R.M.,	"Look-Ahead Prod	cessors," Computing Surveys,	ACM, Vol. 7, No. 4, pp. 1	77-195 (December	1975).	
RLE	AR	<u>5</u>	Lightner, B.D. 1991).	ghtner, B.D. and Hill, G., "The Metaflow Lightning Chipset", Compcon Spring 91, IEEE, pp. 13-18 (February 25 - March 1, 991).					
RIF	AS	5	Patt, Y.N. et d Workshop on	tt, Y.N. et al., "Critical Issues Regarding HPS, A High Performance Microarchitecture", Proceedings of 18th Annual orkshop on Microprogramming, IEEE, pp. 109-116 (December 3-6, 1985).					
RUE	AT	<u>5</u>	Hwu et al.," COMPCON	Experiments with 86, IEEE, pp. 254	HPS, a Restricted Data Flor 1-258 (1986).	w Microarchitecture for l	High Performance	Computers,"	
	Richa		Ellis			1	CONSIDERED	poliulzooy	
EXAMINER: Init and not consider	ial if refer ed. Indu	ence co de copy	nsidered, whe	ther or not citation	n is in conformance with M ication to Applicant.	PEP 609. Draw line thr	ough citation if not	in conformance	

	Page 6 of 10
ATTY. DOCKET NO. SP038.C5 (1397.0140005)	APPLICATION NO. To Be Assigned 101815,742
FIRST NAMED INVENTOR WANG et al.	
FILING DATE April 2, 2004	ART UNIT To Be Assigned

						IIS P	ATENT DOCUMENTS			
EX	AMIN	NER		DOCU	MENT		AIENI DOCUMENTO	· · · · · · · · · · · · · · · · · · ·		F.
	TIAL			NUMB		DATE	NAME	CLASS	SUB-CLASS	FILING DATE
1			AA6				10.000	00.00	1000-01-00	FILING DATE
1								.		1
1	١		AB6	-						
	 			ļ					<u> </u>	
	1		AC6		I			1	T	
	+		AD6				 		 	
	1	- 1	700		1					
	\top		AE3				 	- - - - - - - - - - - - - -	- 	
	\bot]						ļ	
_	1		AF6						-	T
	-+							<u>_</u>		
	1	.]	AG6							
		-+	AH6							
		1	Ano	ı	-				1	1
		1	Al6					- 	 	
		$\Lambda = \Gamma$						į		
		7	AJ6						 	
		\rightarrow						_		
		- \]-	AK6							
		_ \				5005:01				
EY	AMIN	ICD	Τ	TDOC	LIBATAT	FOREIGN	PATENT DOCUMENT	rs		
INIT		IER]	NUM	UMENT	DATE	COUNTRY	01.400		
		T	 	11011	<u>DLIN</u>	- DAIL	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
		1	AL6			1				Yes
		1								No Yes
			AM6							No
		- 1								Yes
			AN6			i .			1	
					OTHER (No
_					OTHER (I	ncluding Aut	hor, Title, Date, Pertin	ent Pages, etc.)		No
~ ·	7.5		40						18th Annual Wow	
F	< v	FE	AO	<u>6</u>	Patt, Y.N. et a	ıl., "HPS, A New]	Microarchitecture: Rationale a	nd Introduction" The	18 th Annual Worl	kr han an
*	<i>₹₽</i>	FE	AO	<u>6</u>	Patt, Y.N. et a	ıl., "HPS, A New]		nd Introduction" The	18 th Annual Worl	kr han an
*	<i>20</i>	E			Patt, Y.N. et a Microprogram	nl., "HPS, A New I	Microarchitecture: Rationale arove, CA, December 3-6, 1985,	nd Introduction", The	ety Order No. 653	kshop on 3, pp. 103-108.
7	ZV ZL	E E	AO AP	6	Patt, Y.N. et a Microprogram Patt et al., "Ru	nl., "HPS, A New Inming, Pacific Gro	Microarchitecture: Rationale a	nd Introduction", The	ety Order No. 653	kshop on 3, pp. 103-108.
7	20 21	E E		6	Patt, Y.N. et a Microprogram Patt et al., "Ru	nl., "HPS, A New Inming, Pacific Gro	Microarchitecture: Rationale as ove, CA, December 3-6, 1985,	nd Introduction", The	ety Order No. 653	kshop on 3, pp. 103-108.
7	20 20	E E	AP	<u>6</u>	Patt, Y.N. et a Microprogram Patt et al., "Rt 19 Workshop,	nl., "HPS, A New Inming, Pacific Groun- nun-Time Generation New York, pp. 75	Microarchitecture: Rationale and ove, CA, December 3-6, 1985, on of HPS Microinstructions Fig. 8-81 (October 1986).	nd Introduction", <i>The</i> IEEE Computer Soci	on Stream," Proce	ishop on B, pp. 103-108. Pedings of MICRO
The Tax	20 20 20	E E	AP	6	Patt, Y.N. et a Microprogram Patt et al., "Rt 19 Workshop, Peleg, A. and	nl., "HPS, A New Inming, Pacific Groun-Time Generation New York, pp. 75	Microarchitecture: Rationale as ove, CA, December 3-6, 1985,	nd Introduction", <i>The</i> IEEE Computer Soci	on Stream," Proce	ishop on B, pp. 103-108. Pedings of MICRO
7	RU RU RU	E E	AP	6	Patt, Y.N. et a Microprogram Patt et al., "Rt 19 Workshop, Peleg, A. and	nl., "HPS, A New Inming, Pacific Groun-Time Generation New York, pp. 75	Microarchitecture: Rationale and ove, CA, December 3-6, 1985, on of HPS Microinstructions Fig. 81 (October 1986).	nd Introduction", <i>The</i> IEEE Computer Soci	on Stream," Proce	ishop on B, pp. 103-108. Pedings of MICRO
The Table of the T	RU RU RU	E E E	AP AR	<u>6</u>	Patt, Y.N. et a Microprogram Patt et al., "Rt 19 Workshop, Peleg, A. and CISC Perform	nl., "HPS, A New Inming, Pacific Groun-Time Generation New York, pp. 75 Weiser, U., "Futuriance Potential", Il	Microarchitecture: Rationale and ove, CA, December 3-6, 1985, on of HPS Microinstructions Fig-81 (October 1986). The Trends in Microprocessors: EEE, pp. 263-266 (1991).	nd Introduction", The IEEE Computer Sociorom a VAX Instruction	on Stream," Proce	ishop on 3, pp. 103-108. redings of MICRO
To The Total Control of the Control	20 21 21	E E E	AP AR	<u>6</u>	Patt, Y.N. et a Microprogram Patt et al., "Rt 19 Workshop, Peleg, A. and CISC Perform Pleszkun, A.R	nl., "HPS, A New Inming, Pacific Groun-Time Generation New York, pp. 75 Weiser, U., "Futuriance Potential", Il	Microarchitecture: Rationale and ove, CA, December 3-6, 1985, on of HPS Microinstructions Fig-81 (October 1986). Te Trends in Microprocessors: EEE, pp. 263-266 (1991).	nd Introduction", The IEEE Computer Soci rom a VAX Instruction Out-of-Order Execut	on Stream," Proce	tshop on 3, pp. 103-108. redings of MICRO
To The Total Control of the Control	20 21 21 21	E E E	AP AR	<u>6</u>	Patt, Y.N. et a Microprogram Patt et al., "Rt 19 Workshop, Peleg, A. and CISC Perform Pleszkun, A.R	nl., "HPS, A New Inming, Pacific Groun-Time Generation New York, pp. 75 Weiser, U., "Futuriance Potential", Il	Microarchitecture: Rationale and ove, CA, December 3-6, 1985, on of HPS Microinstructions Fig-81 (October 1986). The Trends in Microprocessors: EEE, pp. 263-266 (1991).	nd Introduction", The IEEE Computer Soci rom a VAX Instruction Out-of-Order Execut	on Stream," Proce	ishop on 3, pp. 103-108. redings of MICRO
To The Total Control of the Control	20 20 20 20 20	E E E	AP AR AS	<u>6</u>	Patt, Y.N. et a Microprogram Patt et al., "Rt 19 Workshop, Peleg, A. and CISC Perform Pleszkun, A.R 15th Annual S	nl., "HPS, A New Inming, Pacific Groun-Time Generation New York, pp. 75 Weiser, U., "Futur Lance Potential", Il and Sohi, G.S., "Symposium on Con	Microarchitecture: Rationale and ove, CA, December 3-6, 1985, on of HPS Microinstructions Fig. 81 (October 1986). Te Trends in Microprocessors: EEE, pp. 263-266 (1991). The Performance Potential of inputer Architecture, IEEE, pp.	nd Introduction", The IEEE Computer Sociorom a VAX Instruction Out-of-Order Execut Multiple Functional 37-44 (June 1988).	on Stream," Procesion, Speculative B	kshop on B, pp. 103-108. redings of MICRO tranching and their Proceedings of the
To The Total Control of the Control	20 20 20 20 20 20	E E E	AP AR AS	<u>6</u>	Patt, Y.N. et a Microprogram Patt et al., "Rt 19 Workshop, Peleg, A. and CISC Perform Pleszkun, A.R. 15th Annual S. Pleszkun, A.R.	nl., "HPS, A New Inming, Pacific Groun-Time Generation New York, pp. 75 Weiser, U., "Futurance Potential", Illumona Sohi, G.S., "Symposium on Control on	Microarchitecture: Rationale as ove, CA, December 3-6, 1985, on of HPS Microinstructions Fig-81 (October 1986). The Trends in Microprocessors: EEE, pp. 263-266 (1991). The Performance Potential of inputer Architecture, IEEE, pp. 263-266 (1991).	nd Introduction", The IEEE Computer Sociorom a VAX Instruction Out-of-Order Execut Multiple Functional 37-44 (June 1988).	on Stream," Procesion, Speculative B	kshop on B, pp. 103-108. redings of MICRO tranching and their Proceedings of the
<u> </u>	RU	R E	AP AR AS	<u>6</u>	Patt, Y.N. et a Microprogram Patt et al., "Rt 19 Workshop, Peleg, A. and CISC Perform Pleszkun, A.R. 15th Annual S Pleszkun, A.R. Symposium on	nl., "HPS, A New Inming, Pacific Groun-Time Generation New York, pp. 75 Weiser, U., "Futurance Potential", Illumona Sohi, G.S., "Symposium on Control on	Microarchitecture: Rationale and ove, CA, December 3-6, 1985, on of HPS Microinstructions Fig. 81 (October 1986). Te Trends in Microprocessors: EEE, pp. 263-266 (1991). The Performance Potential of inputer Architecture, IEEE, pp.	nd Introduction", The IEEE Computer Sociation a VAX Instruction Out-of-Order Execute Multiple Functional 37-44 (June 1988). Interpretation of the Interpretation of the Ieee Computer Sociation of the Ieee Computer Sociation of the Ieee Computer Sociation of Ieee C	on Stream," Procession, Speculative B	kshop on B, pp. 103-108. redings of MICRO tranching and their Proceedings of the
<u> </u>	RUR RUR	R E	AP AR AS	6 6	Patt, Y.N. et a Microprogram Patt et al., "Rt 19 Workshop, Peleg, A. and CISC Perform Pleszkun, A.R. 15th Annual S. Pleszkun, A.R.	nl., "HPS, A New Inming, Pacific Groun-Time Generation New York, pp. 75 Weiser, U., "Futurance Potential", Illumona Sohi, G.S., "Symposium on Control on	Microarchitecture: Rationale as ove, CA, December 3-6, 1985, on of HPS Microinstructions Fig-81 (October 1986). The Trends in Microprocessors: EEE, pp. 263-266 (1991). The Performance Potential of inputer Architecture, IEEE, pp. 263-266 (1991).	nd Introduction", The IEEE Computer Sociation a VAX Instruction Out-of-Order Execute Multiple Functional 37-44 (June 1988). Interpretation of the Interpretation of the Ieee Computer Sociation of the Ieee Computer Sociation of the Ieee Computer Sociation of Ieee C	on Stream," Procesion, Speculative Bunit Processors,"	kshop on B, pp. 103-108. redings of MICRO tranching and their Proceedings of the

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

	Page 7 of 10
ATTY. DOCKET NO. SP038.C5 (1397.0140005)	APPLICATION NO. To Be Assigned 10/8/5,742
FIRST NAMED INVENTOR	
WANG et al.	LADTUNE
FILING DATE April 2, 2004	ART UNIT
April 2, 2004	To Be Assigned

				U.S. F	ATENT DOCUMENTS					
EXAMINER			UMENT			T				
INITIAL	AA7	NUM	BER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE		
<u> </u>		ļ								
	AB7									
	AC7									
	AD7									
	AE7						-	 		
	AF7	ļ —		1 V						
	AG7					 				
	AH7			•						
	AI7	·	_			7		<u> </u>		
	AJ7									
	AK7									
EVALUED		150		_ FOREIGI	N PATENT DOCUMENTS					
EXAMINER INITIAL	_		CUMENT MBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION		
	AL7							Yes No		
	AM7							Yes		
	AN7		*					No Yes		
<u> </u>	LOW	—	OTHER (I	ncluding Aut	hor, Title, Date, Pertinen	Pages, etc.)	<u> </u>	No_		
RUE	AO	7	1		ow Architecture", IEEE Micro, IE			-73 (June 1991).		
RLE	AP	7	Smith, J.E. and Annual Interna	d Pleszkun, A.R., ational Symposius	"Implementation of Precise Interr m on Computer Architecture, IEEE	upts in Pipelined E, pp. 36-44 (June	Processors," Proce 1985).	edings of the 12th		
RLE	AR	7	Smith, M.D. e (April 3-6, 198	Smith, M.D. et al., "Limits on Multiple Instruction Issue," Computer Architecture News, ACM, No. 2, pp. 290-302 (April 3-6, 1989).						
RUE	AS	7	Sohi, G.S. and Conference Pr 1987).	Sohi, G.S. and Vajapcyam, G.S., "Instruction Issue Logic For High-Performance, Interruptable Pipelined Processors," Conference Proceedings of the 14th Annual International Symposium on Computer Architecture, pp. 27-34 (June 2-5, 1987).						
RUE	AT	<u>7</u>	Thornton, J.E.	, Design of a Con	nputer: The Control Data 6600, Co	ontrol Data Corpo	ration, pp. 57-140	(1970).		
EXAMINER	Richa	ird	Ellis				CONSIDERED	10/14/2004		
EXAMINER: Initi	al if refer	ence co	nsidered, wheth	her or not citation	is in conformance with MPEP 60 ation to Applicant.	9. Draw line thro	ough citation if not	in conformance		
					w r upnount.					

	_	_	_	
Pag	e	8	of	10

FORM PTO-1449

ATTY. DOCKET NO. SP038.C5 (1397.0140005) FIRST NAMED INVENTOR

APPLICATION NO. To Be Assigned

10/815,742

INFORMATION DISCLOSURE STATEMENT

WANG et al. FILING DATE April 2, 2004

ART UNIT To Be Assigned

L					U.S. F	PATENT DOCUME	NTS			
EXAMINE	R			UMENT					Ţ · · · · · · · · · · · · · · · · · · ·	
INITIAL		A A O	NUM	BER	DATE	NAME	CL	_ASS	SUB-CLASS	FILING DATE
1		8AA			:		1			
		AB8	 							
									İ	
	Ĩ	AC8			ļ					
	-	AD8								
		700								
		AE8								
\vdash										
} \		AF8		•		1				
		AG8							ļ	
									1	İ
	$\neg \neg$	AH8								
		AIO								
1 1		Al8								
		AJB				<u> </u>				
1								_		
\		AK3								
	1-				EODEIG	N PATENT DOCUM	AENTO			<u> </u>
EXAMINE	R	1	DO	CUMENT	1 OKLIG	TATENT DOCUM	MENIS -	- i		•
INITIAL		<u></u>	-	MBER	DATE	COUNTRY	lc	LASS	SUB-CLASS	TRANSLATION
/										Yes
	-	AL8	+		-					No
'	1	AM8								Yes
	1		1							No Yes
	1_	AN8								No
				OTHER (Including Aut	thor, Title, Date, Pe	ertinent Page	es, etc.)		
RUE RUE		AO	<u>8</u>	Tjaden, G.S. Computers, I	and Flynn, M.J., " EEE, Vol. C-19, N	Detection and Parallel Ex No. 10, pp. 889-895 (Octo	xecution of Indepo ber 1970).	endent Inst	ructions," IEEE 7	rans. On
<u> </u>				ļ						- · · · · · · · · · · · · · · · ·
VU5		AP	<u>8</u>	Tjaden, G.S., (1972).		nd Detection of Concurre	ency Using Order	ing Matrice	s, (Dissertation),	UMI, pp. 1-199
17.40		-			· · ·					
500	-	45	_	Tiaden et al	"Representation of	of Concurrency with Orde	ering Matrices " I	FFF Trans	actions On Comp	where IEEE Val
1 XU8		AR	<u>8</u>	C-22, No. 8,	pp. 752-761 (Augi	ust 1973).	ring wantes, 7	EEE Transi	ictions On Comp	uters, ieee, vol.
	_		_	 						
DIE	;]	AS	<u>8</u>	Tomasulo, R.	.M., "An Efficient	Algorithm for Exploiting	Multiple Arithm	etic Units.'	' <i>IBM Journal</i> . IB	M. Vol. 11. nn
Pu	_	70	<u>u</u>	25-33 (Januai	ry 1967).		•			, тол тт, рр.
Control of the second of the s								ritorija.	The second secon	
RUE RUE	2	AT	<u>8</u>	Uht, A.K., "A	In Efficient Hardv Hawaii Internation	vare Algorithm to Extract nal Conference on System	Concurrency From Sciences, HICSS	om General S, pp. 41-50	Ршроѕе Code," / (1986).	Proceedings of the
EXAMINE	$\frac{1}{R}$	5 /	1 ,	<u>// '</u>		·				
	t	richo		ellis					ONSIDERED)	0/14/2004
EXAMINER	t: Initia	l if refere	nce co	nsidered, whe	ther or not citation	is in conformance with	MPEP 609. Drav	w line throu	igh citation if not	in conformance

and not considered. Include copy of this form with next communication to Applicant.

		-,
	T	Page 9 of 10
	ATTY. DOCKET NO.	APPLICATION NO.
	SP038.C5 (1397.0140005)	To Be Assigned 10/815,742
	FIRST NAMED INVENTOR	
٠,	WANG et al.	
	FILING DATE	ART UNIT
	April 2, 2004	To Be Assigned

					U.S	. PATENT DOCUMENT	S		
EXAM INITIA	AINER		DOCI	UMENT BER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
		AA9	<u></u>] .		
		AB9							
		AC9							
		AD9				·			
	ı	AE9			<u> </u>				-
		AF9				-			
-		AG9			-			· ·	
	1	AH9	 			-			· · · · · · · · · · · · · · · · · · ·
	+-	Al9		-	 		-	 	
		AJ9							<u> </u>
	+	AK9			<u> </u>			 	
-		l	L		FOREI	GN PATENT DOCUME	MTC		
EXAM	IINER	T	TDO	CUMENT	- OKL	SITTATENT DOCUME	413		
					l - . - -	l		l i	
AITINI				MBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
		AL9			DATE	COUNTRY	CLASS	SUB-CLASS	Yes No
					DATE	COUNTRY	CLASS	SUB-CLASS	Yes No Yes
		AL9			DATE	COUNTRY	CLASS	SUB-CLASS	Yes No Yes No
				MBER					Yes No Yes
		AM9		MBER		COUNTRY .uthor, Title, Date, Perti			Yes No Yes No Yes
AITIMI	NL.	AM9		OTHER Uvieghara,	(Including A	uthor, Title, Date, Perti	inent Pages, etc.)		Yes No Yes No Yes No
AITINI		AM9 AN9	NUN	OTHER Uvieghara, Technical P	(Including A G.A. et al., "An apers, 2 pages (I G.A. et al., "An	uthor, Title, Date, Perti	inent Pages, etc.) Flow CPU," Symposius	m on ULSI Circuit	Yes No Yes No Yes No
AITINI	WE.	AM9 AN9 AO	9	OTHER Uvieghara, 1 Technical P Uvieghara, 4 Vol. 27, No.	(Including A G.A. et al., "An apers, 2 pages (I G.A. et al., "An 1, pp. 17-28 (Ja	Experimental Single-Chip Data May 1990).	inent Pages, etc.) Flow CPU," Symposius Flow CPU," IEEE Jour	m on ULSI Circuit	Yes No Yes No Yes No Yes No Corcuits, IEEE,
TRITINI TO THE TRITINI THE TRITINI TO THE TRITINI TO THE TRITINI THE	WE.	AM9 AN9 AO	9	OTHER Uvieghara, vertical Properties Uvieghara, vol. 27, No. Wedig, R.G. 179 (June 19) Weiss, S. an	(Including A G.A. et al., "An apers, 2 pages (I G.A. et al., "An 1, pp_ 17-28 (Ja ., Detection of C 982).	Experimental Single-Chip Data May 1990). Experimental Single-Chip Data nuary_1992).	inent Pages, etc.) Flow CPU," Symposium Flow CPU," IEEE Journ d Language Instruction	m on ULSI Circuit rnal of Solid-State Streams, (Dissert	Yes No Yes No Yes No Yes No Corcuits, LEEE, Aution), UMI, pp. 1-
TRITINI TO THE TRITINI THE TRITINI TO THE TRITINI TO THE TRITINI THE	WE WE	AM9 AN9 AO AP AR	<u>9</u>	OTHER Uvieghara, Technical P Uvieghara, Vol. 27, No. Wedig, R.G. 179 (June 19) Weiss, S. an Vol. C-33, No.	(Including A G.A. et al., "An apers, 2 pages (I G.A. et al., "An al., 1, pp. 17-28 (Ja , Detection of C 982). and Smith, J.E., "I No. 11, pp. 77-86 et al., "On Tuni	Experimental Single-Chip Data May 1990). Experimental Single-Chip Data nuary 1992). Concurrency In Directly Executed instruction Issue Logic in Pipelii	Flow CPU," Symposium Flow CPU," IEEE Journal A Language Instruction and Supercomputers," I	m on ULSI Circuit rnal of Solid-State Streams, (Dissert	Yes No Yes No Yes No Yes No S Design Digest of Circuits, IEEE, ation), UMI, pp. 1- computers, IEEE,

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

•				Page 10 of 10
		ATTY. DOCKET NO. SP038.C5 (1397.0140005)	APPLICATION NO. To Be Assigned	10/815,742
FORM PTO-1449		FIRST NAMED INVENTOR		
		WANG et al.		
INFORMATION DISCLOSURE	STATEMENT	FILING DATE	ART UNIT	
		April 2, 2004	To Be Assigned	

					J.S. PATENT DOCUMENTS			· · · · · · · · · · · · · · · · · · ·
EXAMINER			UMENT					
INITIAL	AA10	NUM	BER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	المما							
	AB10				,			
	AC10		-				 	
	AD10	-						
	AE10						<u> </u>	
	AF10	<u> </u>		-			 	
	AG10		_	! 				ļ
-	AH10							
	Al10	ļ						
	AJ10	ļ						
\	AK10							
EVALUED		155		FORE	GN PATENT DOCUME	NTS		
EXAMINER INITIAL			CUMENT MBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL10							Yes No
	AM10							Yes No
	AN10							Yes
			OTHER (ncluding A	uthor, Title, Date, Pert	inent Pages, etc.)	<u> </u>	No
RUE	AO	10	Notice of F	Reasons Fo	r Rejection, dated Nover 9128 (3 pages) with Eng	mber 5, 2003, issu	ed in Jananes	e Patent
	AP.	<u>10</u> ·						
	AR	<u>10</u>						· · · · · · · · · · · · · · · · ·
	AS	<u>10</u>						
	AT	<u>10</u>				TA WAR	engalaturgum in an anyim fari	and the second s
EXAMINER	Richa	and i	Ellis				CONSIDERED	oliulzonu
EXAMINER: Initiand not consider	al if refere	ence co	nsidered whet	her or not citat	tion is in conformance with MP inication to Applicant.	EP 609. Draw line thro	ough citation if not	in conformance